Flip chip Assembly with Sub-micron 3D Re-alignment via Solder Surface Tension

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Abstract

We demonstrate experimentally a flip-chip assembly with submicron three-dimensional alignment accuracy. We employ solder surface tension to push the flipped chip into lithographically defined alignment stops. During reflow, surface tension forces of the melted solder can move a chip by more than a hundred microns. We use these motions to obtain self-alignment by constraining the motions to lithographically defined mechanical stops and chip edge butting. This approach is particularly useful in InP laser to Si photonic assemblies, where sub-micron alignment is required for low optical connection loss. In this report, our test vehicles comprise silicon photonic chips and laser placeholder chips made of silicon as well. To enable self-alignment of edge-emitting single-mode lasers, a significant re-alignment range is needed to overcome the laser cleaving tolerance of +/- 15 microns and the low +/- 10 microns placement accuracy of high-throughput pick-and-place tools. We employ in-situ infrared (IR) microscopy to look through the assembled chips during solder induced re-alignment. We show that the self-alignment of the chips starts at the moment the solders melt. Cross sectional analysis is used to confirm the alignment accuracy and contact on the lithographic stops. We discuss process window considerations related to standoff height and solder volume.

Introduction

Silicon photonic technology brings the advantages of semiconductor manufacturing to the production of photonic components for high speed and long distance optical communication [1, 2]. To utilize these advantages, improvements in cost and scalability of Si photonic packaging is needed. Several packaging steps are required for connecting a nanophotonic chip to a light source (laser) and optical fibers. Our team has reported on cost effective interfacing between Si nanophotonic chips and optical fibers in ECTC 2014 [3].

A fundamental issue in photonic components is the accurate positioning and there are reports which show passive assembly for laser modules using the self-alignment of solders with mechanical stops [4-7]

Our goal is to use edge facet laser chips and optical alignment between a laser chip and a nanophotonic chip, which requires sub-micron accuracy in three dimensions. There are therefore substantial challenges to overcome in using solder reflow for edge facet laser assembly on Si nanophotonic chips. The sample/material/process need to have the following characteristics:

(1) The packaging method must accommodate the cleaving or dicing tolerance of the laser chip. Although each chip has different distance from the alignment marks to the chip edge due to the chip cleaving or dicing tolerance, the edge of the laser chip where light comes from has to contact the waveguides of Si photonic chips after the assembly. A cleaved laser chip has a size tolerance of +/- 15 microns.

(2) The final alignment accuracy between laser flipped chip and Si photonic substrate chip must be submicron, commensurate to single-mode optics, despite the low +/- 10 microns alignment accuracy capability of high speed pick & place tools .

(3) New materials are required to make good solder interconnection without liquid type flux because flux residue and outgassing are not compatible with good optical performance. Furthermore, chips should not be moved by the vibration of belts in reflow tools when no liquid flux is used.

(4) The solder amount and the gap between a chip and a substrate are key parameters that must be tightly controlled. The gap (and hence the amount of solder) is critical to generate the correct amount of self-alignment force during solder reflow.

In this paper, we report on flip chip assemblies with three-dimensional re-alignment using solder surface tension and lithographically defined stops. To achieve a cost-effective packaging method along with high yield, we focus on processes and tooling currently found in semiconductor manufacturing environments such as high-throughput pick & place tools and belt reflow furnaces instead of a high accuracy flip-chip bonders.

Experiments

Our target is to enable standard high-speed pick & place tooling followed by standard solder reflow for high-accuracy flip chip assembly. Our work aims at InP laser flip-chip assembly to Si nanophotonic chips but can be applied to any flip-chip assembly requiring high alignment accuracy. Therefore, to facilitate our work, our test vehicles were made of silicon with lithographic defined mechanical structures, and comprise silicon photonic chips (also called substrates) and laser placeholder chips.

Figure 1 (a) and (b) show optical microscope images of a chip and a substrate used for achieving XYZ direction self-alignment with submicron accuracy. The size of a chip is 2.3 x 0.6 mm where one chip has 54 pads which are 114 x 55 um in size each pad. Under bump metallurgy (UBM) of the chip pads is 1 μm Ni/0.2 μm Cu/0.1 μm Au. There was no solder plated on the chip pads. As shown in Figure 1 (a), there is a mechanical stop on the chip for Y direction alignment. The size of mechanical stop on the chip is 50 μm wide and 215 μm long. Figure 1 (b) shows the substrate with a recessed cavity, 8 waveguides, and 5 standoffs as well as 54 solder bumped pads. The substrate pads are matched to the chip pads. Sn-0.6wt%Ag solders were deposited on the pads of the substrate by electroplating method. We experimented with a thickness of electroplated solder ranging from 5 to 15 um. Including the

UBM on both sides, the total metal height was between 8 and 18 um. There are 5 standoffs in the cavity of the substrate. Four out of five standoffs are 30 x 30 μm and serve for Z direction alignment only. One of the 5 standoffs is a little bigger, 50 x 50 μm, and serves as a standoff and a mechanical stop for the Y direction alignment by butting with the mechanical stop on the flipped chip. As discussed below, the standoffs need be slightly higher than the total metal height for optimal performance. The standoff and metal height was adjusted in tandem in our devices. Figure 1 (c) shows the SEM image of the tilted view of dielectric stacks with embedded single-mode waveguides on the substrate side. They are fabricated using lithography and reactive ion etching (RIE) and the X direction self-alignment is achieved by the flipped-chip edge butting into these waveguides.

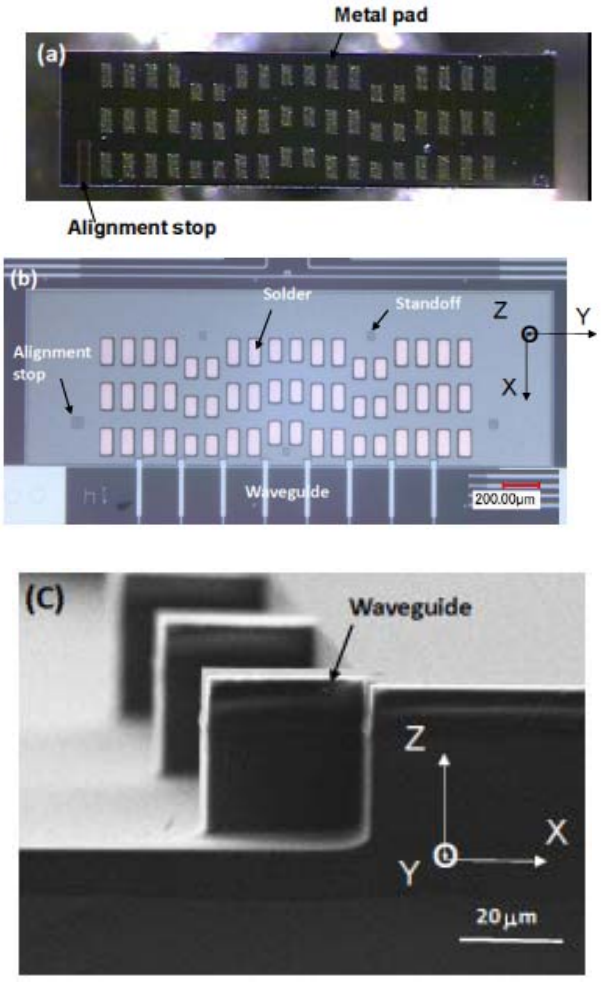

Figure 1. (a) Top view of a test chip, (b) top view of a test substrate, and (c) side view of waveguides on the substrate.

During the Pick & Place, the chip pads and the substrate pads are misaligned intentionally in the XY directions to overcome dicing and tool alignment tolerances. One must ensure that the lateral stops are positioned next to each other prior to reflow and not one on top of each other. The height of the standoffs is larger than that of the electroplated solder, so the flipped-chip surface touches the substrate standoffs when the chip is placed on the substrate. During the reflow, solders pads ball-up, molten solder on the substrate side touches the flipped-chip pads, and wets them. As the pads are offset, this induces flipped-chip movement to minimize the surface energy of the molten solder. The chip movement butts the lateral marks completing the self-alignment. A vapor phase flux is used to remove Sn oxide while avoiding flux residue.

We have assembled an Infra-Red transmission microscope (with IR camera and objective) to view test chips and substrates in transmission. Since silicon is transparent in the IR, we are able to view the chip and substrate pads, as they overlap before and after solder bonding. We are able to view alignment down to a couple microns. In-situ IR transmission microscopy of test-chip over substrate, before and after reflow, was investigated. Only the metal pads of chip and substrate are visible. The picture size is 500 x 500 um approximately.

Results and Discussion

In this study, we made three different types of samples to check how much the accuracy of self-alignment is changed with and without mechanical stops and standoffs.

(1) Full self-alignment without mechanical stops

Figures 2 (a) shows Infrared (IR) camera images from the backside of a chip which was placed on a substrate. The chip pads and the substrate pads are intentionally misaligned by more than a half of each pad in XY directions. This is a maximum misalignment without touching the neighboring pads and the misalignment is more than a hundred microns. After solder reflow in formic acid environment by using self-alignment without any stops, as shown in Figure 2 (a), it is clearly shown that all pads of chip and substrate come to total overlap and aligned well. The movement of the chip started just when solders melting and the self-alignment was finished within a couple of seconds. The movement of the chip during solder reflow was recorded by a movie. Since vapor phase formic acid is used, there is no flux residue recognized in the IR image.

(2) YZ-direction self-alignment using chip edge butting and standoff

Figure 3 (a) and (b) show IR images before and after solder reflow using the chip edge butting into waveguides as Y direction alignment. To check the mechanical stop at the Y direction, the initial intentional misalignment of Y direction is much larger than that of X direction as shown in Figure 3 (a). The bright pads are solder plated substrate pads on the bottom side and the dark pads are chip pads on the top side. After the solder reflow in formic acid, the IR image of Figure 3 (b) clearly shows that there is total overlap of the pads in X direction due to no mechanical stop, however in Y direction, the chip pads did not overlap the substrate pads even though there was movement of the pads in the X direction. The chip moved in X direction until it was stopped by the mechanical contact.

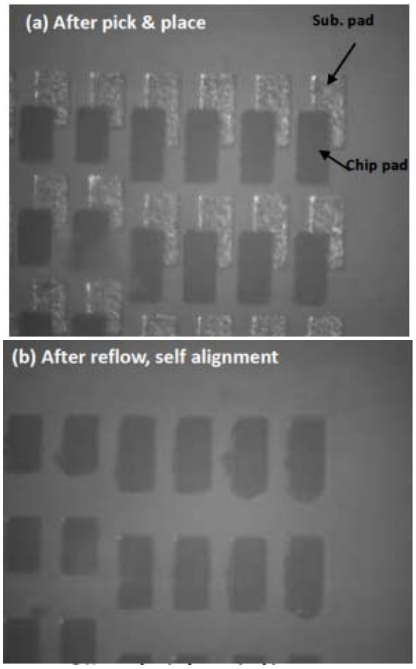

Figure 2. Infrared microscope images of (a) after pick & place and (b) after solder reflow when there is no mechanical stop.

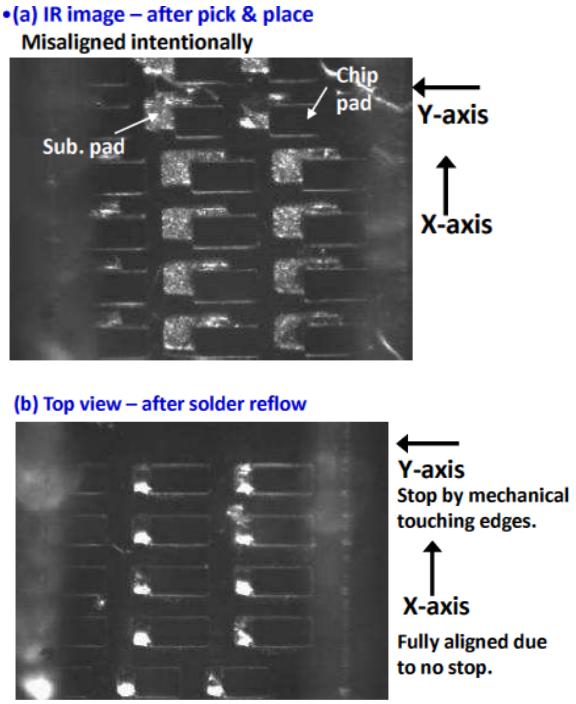

Figure 3. Infrared microscope images of (a) after pick & place and (b) after solder reflow when there is X axis mechanical stop only.

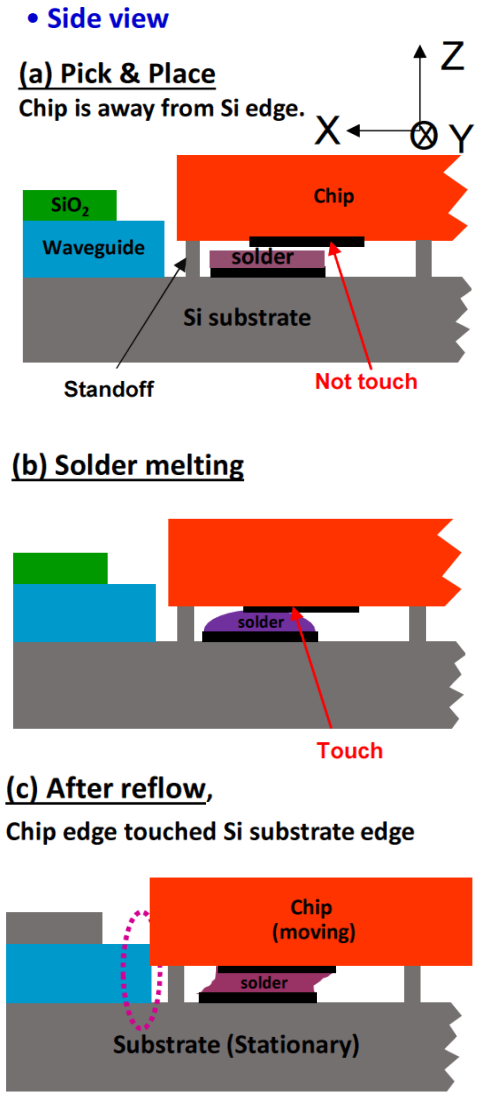

Figure 4. Schematic diagrams of test vehicles (a) after pick & place, (b) solder melting, and (c) after finishing solder reflow.

Figure 4 shows schematic diagrams of the test vehicles after pick & place, solder melting, and after reflow, respectively. As shown in Figure 4 (a), the chip is placed away from the edge of waveguides considering the tolerance of chip dicing or chip cleaving as well as the tolerance of the pick & place tool. As mentioned earlier, a cleaved chip has a size tolerance of +/- 15 microns and a pick and place too has an alignment accuracy of +/- 10 microns. In the worst case, there would be +/- 25 microns tolerance only from these two parameters. Therefore, the pads of a chip have to be intentionally misaligned by more than 25 microns from the edge of a substrate pads. However, the chip pad should not be totally away from the substrate pad because some amount of solder is required to start wetting on the chip pads. In addition, if there is overlapping with neighbored pads, it creates solder bridging. Furthermore, Figure 4 (a) shows the surface of the flipped-chip touching the standoffs on the

substrate after pick & place because the electroplated solder height on the substrate pads is smaller than the standoff height. When solder melts during the reflow process, the flat shape changes into a dome which contacts the chip pads as shown in Figure 4 (b). Following contact, the solder starts to wet and to spread on the chip pads. Then, the surface tension of molten solders make the chip move in the X direction to reduce solder surface area until it is stopped by the edge of the chip touching the waveguides on the substrate. The movement of the chip and the alignment results depend on frictional forces between the chip surface and the top surface of the standoffs. Therefore, it is very important to end up in a clean surface of the standoffs at the end of the fabrications steps, which include deep RIE, solder electroplating, and seed layer etching.

Figure 5 shows an optical microscope image in perspective view and SEM images after the solder reflow process. The chip edge perfectly contacts on all 8 waveguides in the substrate without any gap between the chip edge and waveguides on the substrate. In Figure 6, SEM images of the cross section through the standoff shows that the surface of the chip perfectly contacts on the standoff on the substrate. Based on the information in Figures 5 and 6, it is confirmed that Y and Z direction alignment was successfully achieved by this method.

(3) XYZ-direction self-alignment using chip edge butting a mechanical stop, and stand offs

Our goal is the successful demonstration of self-alignment in all three XYZ directions with submicron accuracy. The alignment stop on the surface of the chip in Figure 1 (a) helps to achieve the mechanical stop of the X direction in addition to the YZ direction as described in Figures 5 and 6. Figure 7 shows an IR image of top view and a SEM image of cross sectional view when the alignment stop on the chip touches the alignment top on the substrate. The alignment stop on the substrate is also working as the standoff for the Z direction alignment. Therefore, the height of the alignment stop on the substrate has to be same height as the other four standoff as shown in Figure 1 (b) even though the area of it is much bigger than the other standoff.

As shown in Figure 7 (a), it can be seen that there is a still an offset between the chip pads and the substrate pads after the solder reflow. However, it is clearly shown that the pads are wetted by the solders and the alignment stop of the chip perfectly contacts with the alignment stop of the substrate. The leftover offset between chip and substrate pads is by design to warrant that the re-alignment force will not subside prior to butting. In Figure 7 (b), a cross sectional SEM shows that the alignment stops of chip/substrate contact well with each other and the surface of the chip contacts on the top of alignment stop/standoff of the substrate. Therefore, Figure 7(b) proves that alignment of the YZ direction has been successfully done with submicron accuracy. The X direction alignment of this sample was confirmed by checking the chip edge butting on 8 waveguides of the substrate before the cross section.

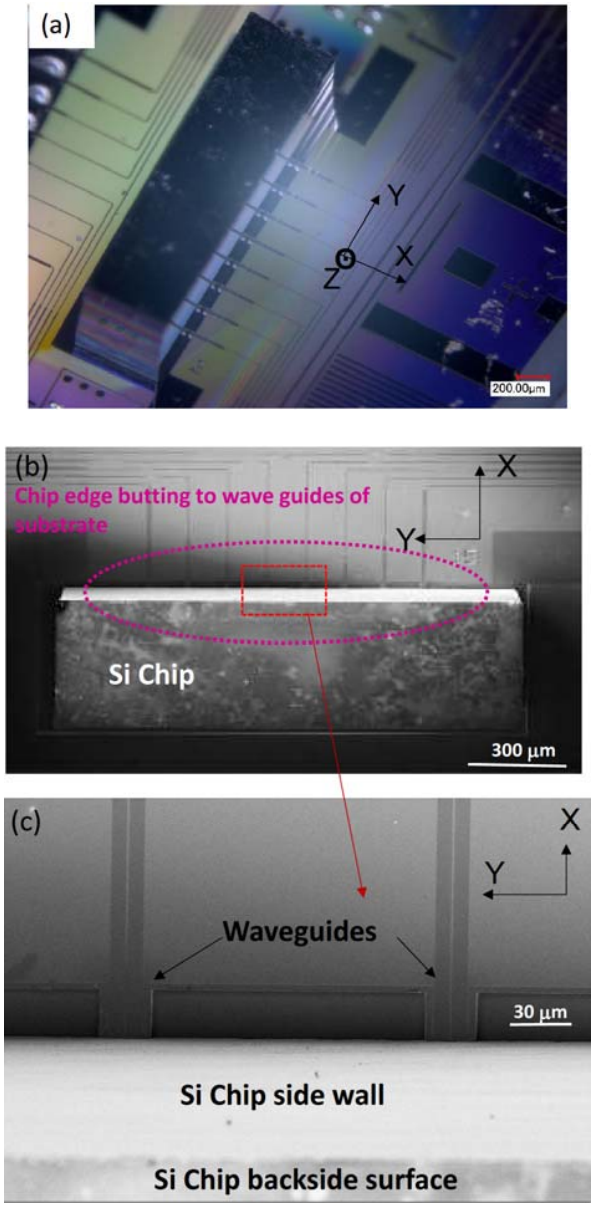

Figure 5. (a) Optical micrograph in perspective view and (b) SEM image of flip chip assembled a chip on a substrate, (c) SEM image of chip side wall touches on the waveguide of the substrate.

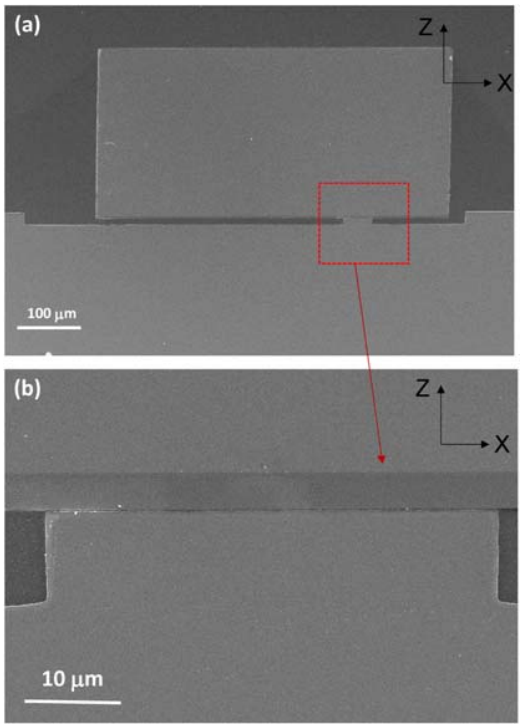

Figure 6. Cross sectional SEM images after solder reflow. The surface of a chip directly contact on the standoff of a substrate.

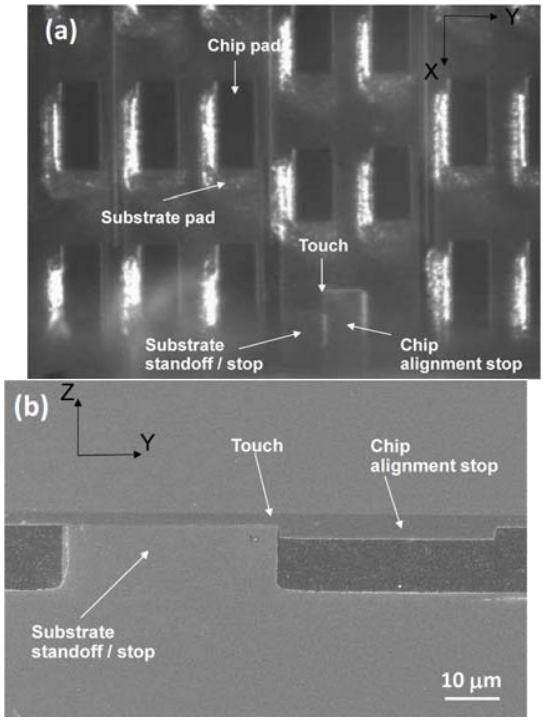

Figure 7. (a) IR image of top view and (b) SEM image of cross sectional view when the alignment stop on the chip touches on the alignment top on the substrate.

Figure 8 shows schematic diagrams of how the YZ direction alignment works from solder surface energy minimization during the reflow process.

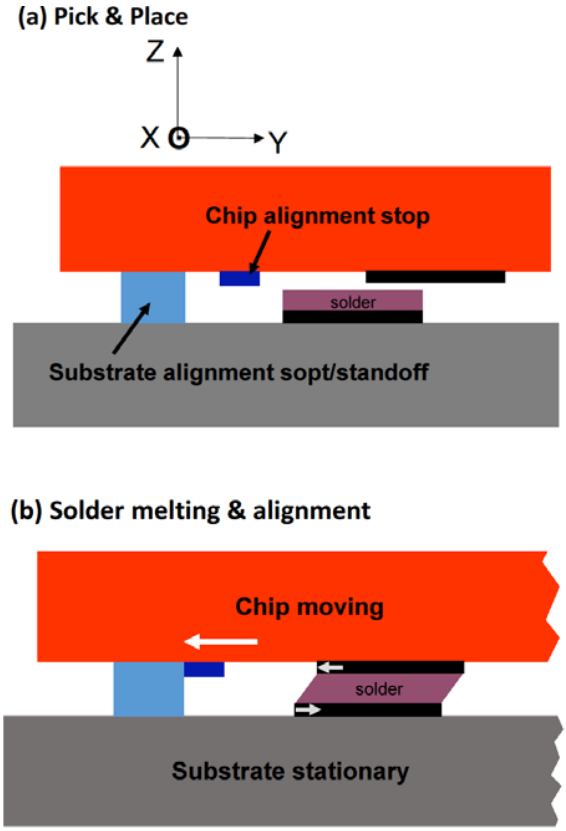

Figure 8. Schematic diagrams of test vehicles (a) after pick & place and (b) solder melting and alignment to the YZ direction.

(4) Self-alignment vs. solder volume

Compared to 1D self-alignment (in X, Y, or in Z direction only), 2D (YZ directions) and 3D (XYZ direction) self-alignment has a much narrower process window so all parameters have to be considered carefully. We have modeled the lateral and vertical surface tension forces of the solder as a function of the amount of the solder between chip and substrate. Our model takes into account the changing curve of the solder surface between chip and substrate as shown in Figure 9. The electroplated solder height needs to be smaller than the vertical standoffs height for the melted solder to pull the flipped chip down at self-alignment. The substrate solder balls up and wets the chip pads only when melted. We found that the gap between the unmelted solder and the flipped chip is a critical parameter. It is related to the amount of solder needed to generate the correct amount of force. At large gaps (or small amount of solder), the lateral force decreases while at small gaps (or large amount of solder), the vertical force decreases. The combined diagrams give us a good assessment of the current process window for the required solder gap, which is about +/- 0.5 um. For a 10 um pad height, this corresponds to a ~5% thickness control at electroplating, which is a little tight as 10% control is more common. We are currently exploring solutions to extend the fabrication process window. A cross sectional image of solder joints in Figure 9 (c) shows an ideal shape of solder joints.

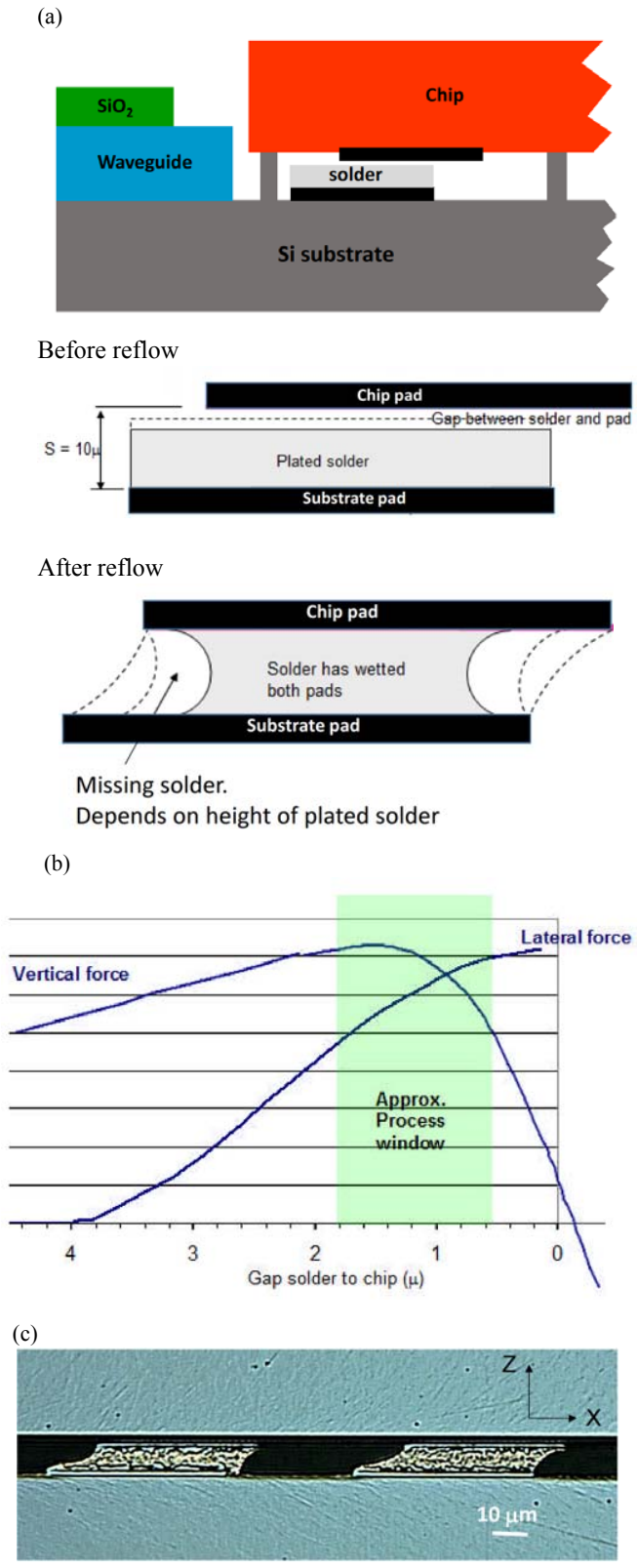

Figure 9. Effect of solder volume on the self-alignment and ideal solder joint shape. (a) Schematic diagram of solder shape before and after reflow, (b) Approximate process window considering vertical and lateral forces from the gap solder to chip, and (c) cross sectional image of solder joint after reflow with mechanical stops.

Conclusions

Flip chip assembly using Sn-0.6wt%Ag solder self-alignment, mechanical stops, and standoffs was experimentally demonstrated with XYZ three dimensional alignment with submicron accuracy. To use an edge facet laser and a high speed pick & place tool, the chip and the substrate were designed to overcome more than 25 microns tolerance of intentional misalignment. During solder reflow, the movement of a chip starts at solder melting and the self-alignment is complete within a second. The chip movement was stopped by a contact between the edge of the chip and waveguides of the substrate in the X direction and by a contact between lithographic alignment stops of chip/substrate in the Y direction. The contact between the chip surface and the stand-offs on the substrate demonstrated Z direction alignment. The approach demonstrated here enables existing high-throughput pick & place tools with high-throughput belt reflow tools to be used for laser flip-chip assembly to Si photonics chips with submicron accuracy.

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